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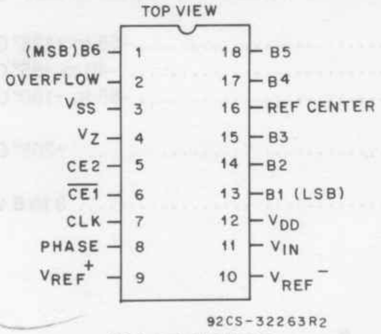
CA3306A, CA3306, CA3306C

Linear Integrated Circuits



18-Lead Package
TERMINAL ASSIGNMENT

CMOS Video-Speed 6-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:
- *CMOS low power with video speed*
- *Parallel conversion technique*
- *Single power supply voltage (3 to 7.5 V)*
- *15-MHz sampling rate with single 5-V supply*
- *6-bit latched 3-state output with overflow bit*
- *Pin-for-pin retrofit for the CA3300*

The RCA-CA3306 family are CMOS parallel (FLASH) analog-to-digital converters designed for applications demanding both low-power consumption and high-speed digitization. Digitizing at 15 MHz, for example, requires only about 50 mW.

The CA3306 family operates over a wide, full-scale signal input-voltage range of 1 volt up to the dc supply voltage. Maximum power consumption is as low as 15 mW, depending upon the clock frequency selected. The CA3306 types may be directly retrofitted into CA3300 sockets, offering improved linearity at a lower reference voltage and higher operating speed with a 5-volt supply.

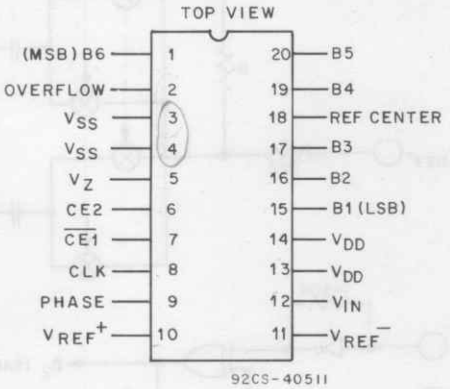
The intrinsic high conversion rate makes the CA3306 types ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3306s in series to increase the resolution of the conversion system. A series connection of two CA3306s may be used to produce a 7-bit high-speed converter. Operation of two CA3306s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz).

Sixty-four paralleled auto-balanced comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3306. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

The CA3306 types are available in an 18-lead dual-in-line ceramic package (D suffix), in an 18-lead dual-in-line plastic package (E suffix), and in a 20-lead dual-in-line small-outline package (M suffix). The CA3306 types are also offered with the additional advantage of improved reliability as a result of the Enhanced Products Program. For further information, see RCA publication EHB-175 or contact your RCA representative.

Applications:
- *The CA3306 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*
- *Robot vision*

TERMINAL ASSIGNMENT



20-Lead Small-Outline Package

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Supersedes issue dated 2-86

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ELECTRICAL CHARACTERISTICS @ $T_A = 25°C$, $V_{DD} = 5$ V, $V_{REF}^+ = 4.8$ V, $V_{SS} = V_{REF}^- =$ GND
Clock = 15 MHz Square Wave for CA3306 or CA3306A, 10 MHz for CA3306C

CHARACTERISTIC		TEST CONDITIONS @ 25°C/NOTES	LIMITS			UNITS
			Min.	Typ.	Max.	
Resolution			6	—	—	Bits
Integral Linearity Error	3306, 3306C	Refer to Figs. 3 and 4	—	±1/4	±1/2	LSB
	3306A		—	±1/5	±1/4	
Differential Linearity Error	3306, 3306C	Refer to Figs. 3 and 4	—	±1/4	±1/2	
	3306A		—	±1/5	±1/4	
Quantizing Error		Inherent	—	—	±1/2	
Offset Error	3306, 3306C	Note 1	—	±1/2	±1	
	3306A		—	±1/4	±1/2	
Gain Error	3306, 3306C	Note 2	—	±1/2	±1	
	3306A		—	±1/4	±1/2	
Positive Full Scale Input Range		Note 3	1	4.8	V_{DD}+0.5	V
Negative Full Scale Input Range		Note 3	-0.5	0	V_{DD}-1	
Input Capacitance			—	15	—	pF
Input Current		Refer to Figs. 5 and 6	—	—	±500	μA
Resistor Ladder Impedance			850	1100	1550	Ω
Maximum Conversion Speed	3306C	Refer to Fig. 7	10	13	—	MSPS
	3306, 3306A		15	20	—	
Maximum Conversion Speed	3306C	$\phi1, \phi2 \geq$ Minimum (not square wave)	12	—	—	
	3306, 3306A		18	—	—	
Auto Balance Time ($\phi1$)	3306C		50	—	∞	ns
	3306, 3306A		33	—	∞	
Sample Time ($\phi2$)	3306C		33	—	5000	
	3306, 3306A		22	—	5000	
Aperture Delay			—	8	—	
Aperture Jitter			—	100	—	ps_{p-p}
Allowable Input Bandwidth			DC	—	$f_{CLOCK}/2$	MHz
-3-dB Input Bandwidth			—	30	—	
Output Data Valid Delay (T_D)	3306C		—	35	60	ns
	3306, 3306A		—	30	45	
Output Data Hold Time	(T_H)		15	25	—	
Output Enable Time	(T_{EN})		—	20	—	
Output Disable Time	(T_{DIS})		—	15	—	
I_{DD} Current	3306C	Refer to Fig. 8	—	11	20	mA
	3306, 3306A		—	14	25	
I_{DD} Current		Continuous $\phi1$	—	7.5	15	
Maximum V_{IN}, Logic 0		All Digital Inputs	—	—	0.3xV_{DD}	V
Minimum V_{IN}, Logic 1		All Digital Inputs	0.7xV_{DD}	—	—	
Digital Input Current		Except CLK	—	±1	±5	μA
Digital Input Current		CLK	—	±100	±200	
Digital Output 3-State Leakage		V_{OUT} = 0 to 5 V	—	±1	±5	
Digital Output Source Current		V_{OUT} = 4.5 V	4	—	—	mA
Digital Output Sink Current		V_{OUT} = 0.4 V	4	—	—	
Zener Voltage		I_Z = 10 mA	5.4	6.2	7.4	V
Zener Dynamic Impedance		I_Z = 10 mA	—	12	25	Ω
Gain Temperature Coefficient			—	+0.1	—	mV/°C
Offset Temperature Coefficient			—	-0.1	—	
Zener Temperature Coefficient			—	-0.5	—	

Notes:
1. OFFSET ERROR is the difference between the input voltage that causes the 00 to 01 output code transition and $(V_{REF}^+ - V_{REF}^-)/128$.
2. GAIN ERROR is the difference between the input voltage that causes the $3F_{16}$ to overflow output code transition and $(V_{REF}^+ - V_{REF}^-) \times 127/128$.
3. The total input voltage range, set by V_{REF}^+ and V_{REF}^-, may be in the range of 1 to $(V_{DD} + 1)$ volts.

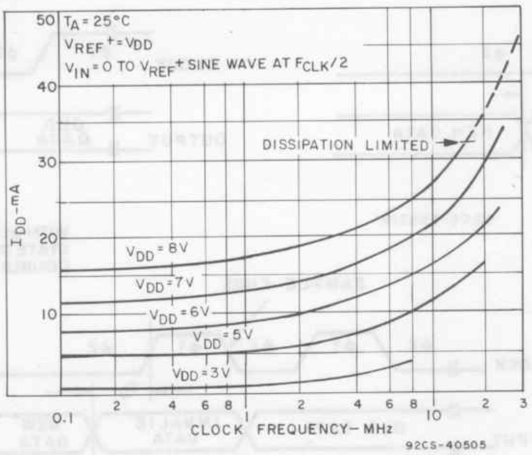


Fig. 8 - Typical I_{DD} as a function of V_{DD}.

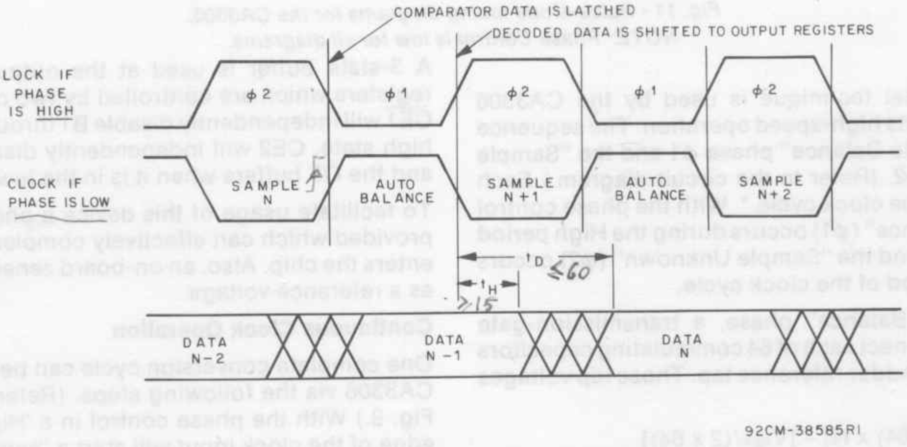


Fig. 9 - Input-to-output timing diagram for CA3306.

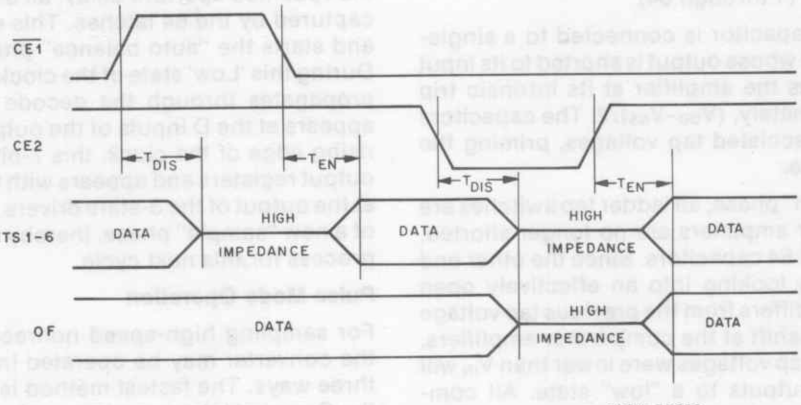


Fig. 10 - Output enable timing diagram for CA3306.

The second method uses the Auto Balance phase, $\phi1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi2$ pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes slightly longer, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of $\phi2$ to $\phi1$. (See timing diagram Fig. 11b.)

For applications requiring both indefinite standby and lowest power, standby can be in the $\phi2$ (Sample Unknown) state with two $\phi1$ pulses to generate valid data (see Fig. 11c). Valid data now appears two full clock cycles after starting the conversion process.

Analog Input Considerations

The CA3306 input terminal is characterized by a small capacitance (see Specifications) and a small voltage-dependent current (see Fig. 6). The signal-source impedance should be kept low, however, when operating the CA3306 at high clock rates.

The CA3306 outputs a short (less than 10 ns) current spike of up to several milliamperes amplitude (see Fig. 5) at the beginning of the sample phase. (To a lesser extent, a spike also appears at the beginning of auto balance.) The driving source must recover from the spike by the end of the same phase, or a loss of accuracy will result.

A locally terminated 50 or 75-ohm source is generally sufficient to drive the CA3306. If gain is required, a high-speed, fast-settling op amp, such as the RCA CA3450, is recommended.

Digital Input and Output Interfacing

The two chip-enable and the phase-control inputs are standard CMOS units. They should be driven from less than 0.3 x V_{DD} to at least 0.7 x V_{DD}. This can be done from 74HC series CMOS (QMOS), TTL with pull-up resistors, or, if V_{DD} is greater than the logic supply, open collector or open drain drivers plus pull-ups.

The clock input is more critical to timing variations, such as $\phi1$ becoming too short, for instance. Pull-up resistors should generally be avoided in favor of active drivers. The clock input may be capacitively coupled, as it has an internal 50-kΩ feedback resistor on the first buffer stage, and will seek its own trip point. A clock source of at least 1 V_{p-p} is adequate, but extremely non-symmetrical waveforms should be avoided.

The output drivers have full rail-to-rail capability. If driving CMOS systems with V_{DD} below the V_{DD} of the CA3306, a CD74HC4050 or CD74HC4049 should be used to step down the voltage. If driving LSTTL systems, no step-down should be necessary, as most LSTTLs will take input swings up to 10 to 15 volts.

Although the output drivers are capable of handling typical data bus loading, the capacitor charging currents will produce local ground disturbances. For this reason, an external bus driver is recommended.

Increased Accuracy

In most cases the accuracy of the CA3306 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the V_{REF}^- input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN}\ (0\text{ to }1\text{ transition}) = \tfrac{1}{2}\text{ LSB} = \tfrac{1}{2}(V_{REF}/64) = V_{REF}/128$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50-ohm pot connected between V_{REF}^- and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50-ohm pot should be connected between V_{REF}^- and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is ½ LSB less than V_{REF}^+ and is calculated as follows:

$$V_{IN}\ (63\text{ to }64\text{ transition}) = V_{REF} - V_{REF}/128 = V_{REF}\ (127/128)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF}^+ until that transition occurs on the outputs.

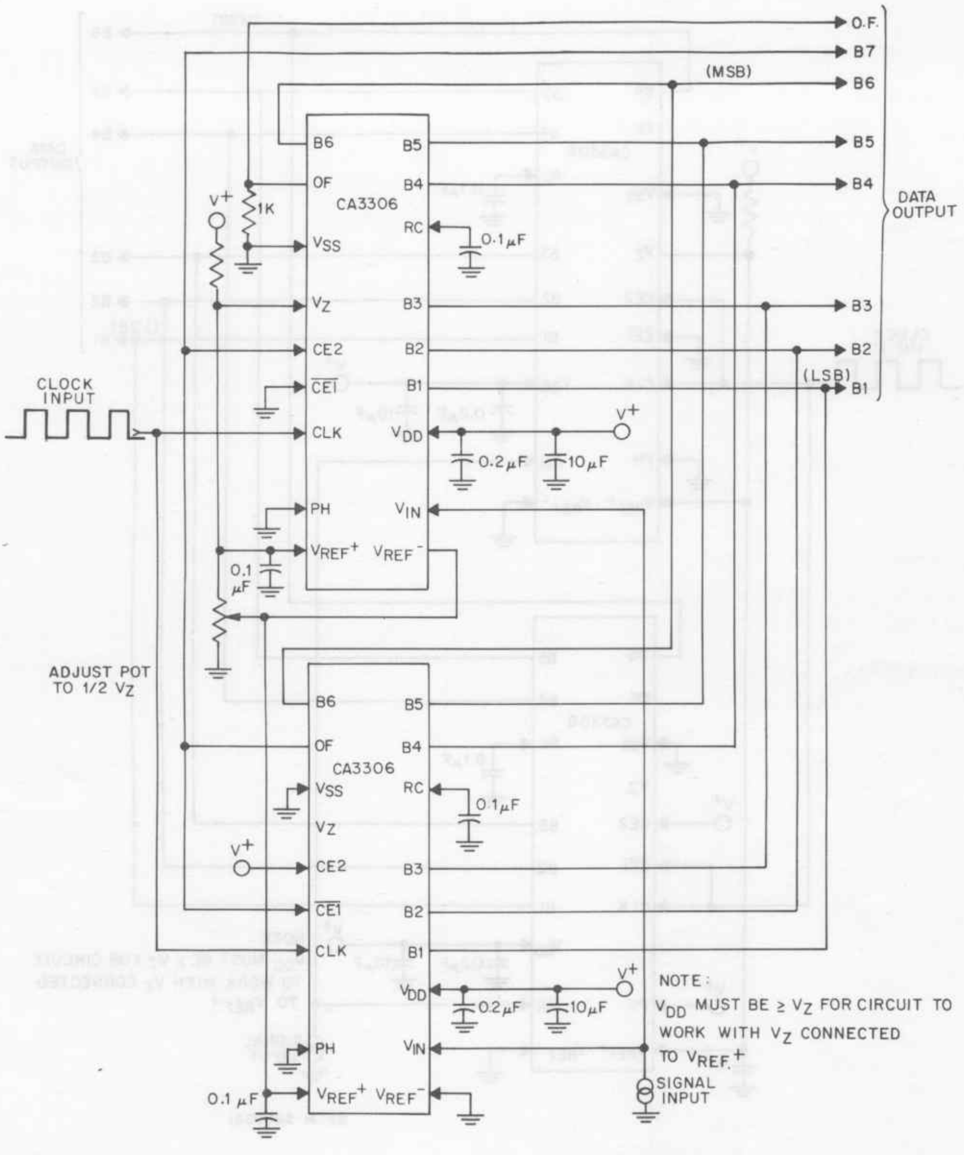
Midpoint Trim

The reference center (RC) is available to the user as the midpoint of the resistor ladder. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 31 to 32 occurs at 31½ LSB's. That voltage is as follows:

$$V_{IN}\ (31\text{ to }32\text{ transition}) = 31.5\ (V_{REF}/64) = V_{REF}\ (63/128)$$

An adjustable voltage follower can be connected to the RC pin or a 2-K pot can be connected between V_{REF}^+ and V_{REF}^- with the wiper connected to RC. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create unique transfer functions. The user must remember, however, that there is approximately 120-ohm in series with the RC pin. This differs from the CA3300, which has a low impedance connection to RC and which actually provides Reference Center + 1 LSB.



NOTE: V_{DD} MUST BE ≥ V_Z FOR CIRCUIT TO WORK WITH V_Z CONNECTED TO V_{REF}^+

Fig. 13 - Typical CA3306 7-bit resolution configuration.

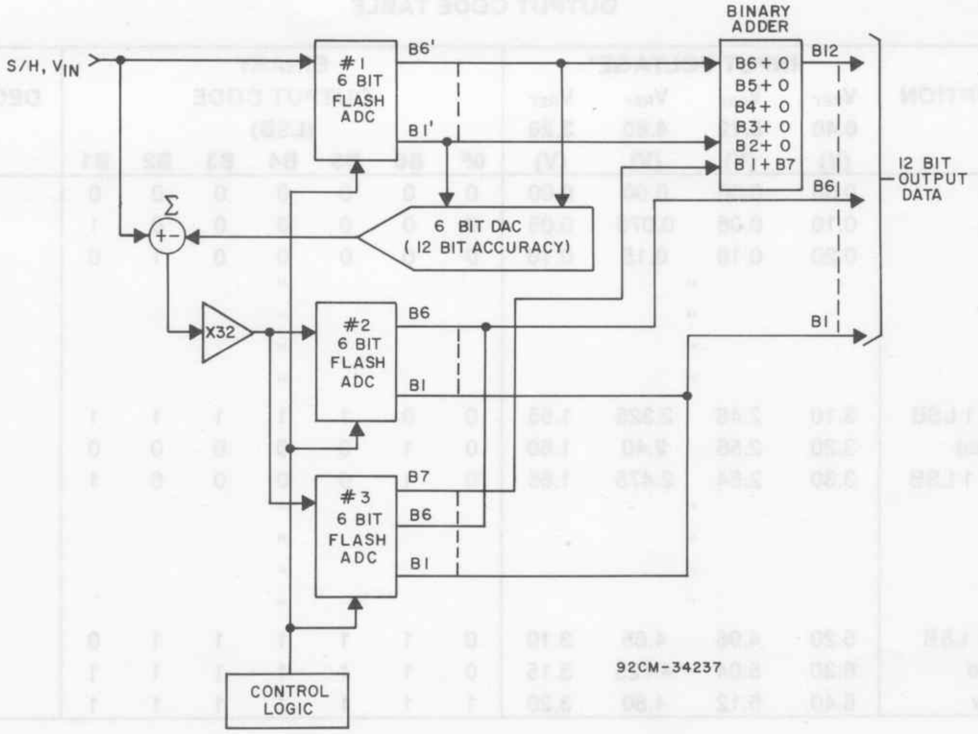


Fig. 15 - Typical CA3306 800-ns, 12-bit ADC system.

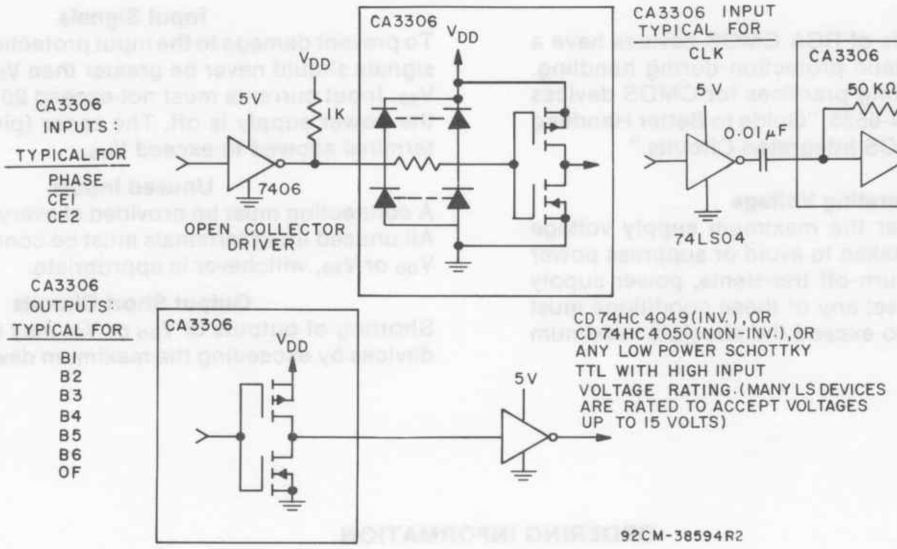
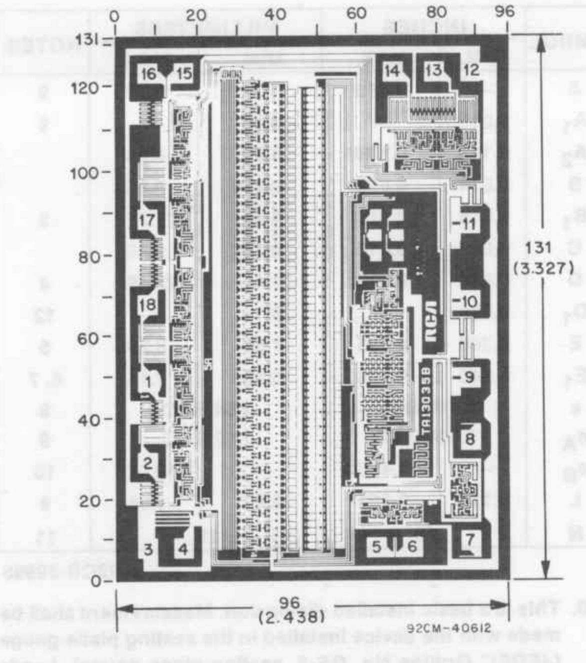


Fig. 16 - Five-volt logic interface circuit for $V_{DD} > 5.5$ volts.



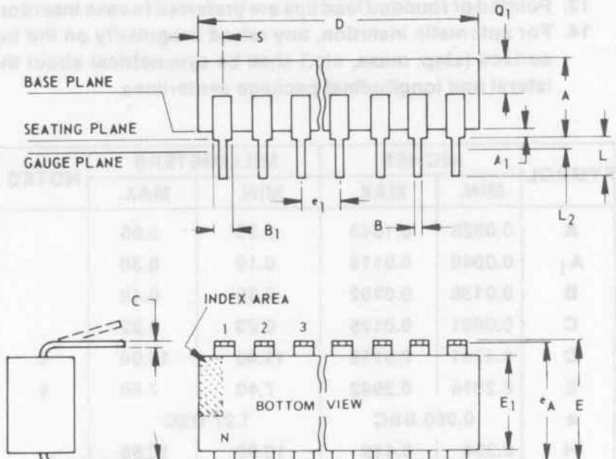
The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Scale graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CA3306H.

DIMENSIONAL OUTLINES

D-Suffix
18-Lead Dual-In-Line Side-Brazed Ceramic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.160	3.05	4.06	
A_1	0.020	0.065	0.51	1.65	
B	0.014	0.020	0.356	0.508	
B_1	0.050	0.065	1.27	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.000	0.76	
α	0°	15°	0°	15°	4
N	18		18		5
N_1	0		0		6
Q_1	0.050	0.085	1.27	2.15	
S	0.015	0.060	0.39	1.52	

92CS-40039

NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. **When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".**
2. **Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.**
3. **e_A applies in zone L_2 when unit installed.**
4. **α applies to spread leads prior to installation.**
5. **N is the maximum quantity of lead positions.**
6. **N_1 is the quantity of allowable missing leads.**